REMARKS

We are in receipt of the Office Action dated February 19, 2003, and the above Amendment and following remarks are made in light thereof.

Claims 1-7, 15-28, 30, 31, 33-42, 44, 45, 51-57 and 64-84 are pending in the application. Pursuant to the Office Action, claims 6, 21, 28 and 35-37 are rejected under 35 U.S.C. 112. Claim 64 is rejected under 35 U.S.C. 112. Claims 5, 22, 23, 26-28, 37 and 57 are rejected under 35 U.S.C. 102(e) as being anticipated by Hamada 6,114,715. Claims 1-4, 6, 7, 15, 16, 18-21, 30, 33, 35-37, 39-42, 44, 51, 53-56 and 65-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamada in view of Wolf, "Silicon Processing for the VLSI Era" in view of Kobayashi, et al., 6,191,183

Turning first to the rejections under 35 U.S.C. 112, the Examiner contends, with respect to claims 6, 21, 28 and 35-37, that although these claims recite that the surface was planarized be flushed, there is no planarization process shown in the specification. Further, the Examiner asserts that the surface is not flush, since it is shown as being as high as 1 micron.

However, in accordance with the present invention, an exposed surface of the protective portion formed in a hole of a pixel electrode is flush with an exposed surface of the pixel electrode by etching, as shown in page 37, lines 5-9 in connection with the description of Embodiment 2. Therefore, Applicant submits that the Examiner's rejection should be withdrawn.

Claim 64 was rejected under 35 U.S.C. 112 for depending upon a claim, claim 11, which had been cancelled. In response, Applicant is canceling claim 64.

Claims 5, 22, 23, 26-28, 37 and 57 have been rejected under 35 U.S.C. 102(e) as being anticipated by Hamada. Claims 5 and 22 are the only independent claims in this group. With respect to claims 5 and 22, the Examiner contends that Hamada shows switching elements 43

with an insulating layer to (column 5, line 32) between pixel electrodes 103 with a third electrode 108. Claims 5 and 22 have been amended to recite that the thickness of a portion of the insulating layer higher than a top surface of the pixel electrode is 0.1 to 1μm. This feature is disclosed on page 12, lines 12-14 of the specification. This feature is not found in Hamada. Consequently, Applicant believes that claims 5 and 22, as amended are no longer anticipated by Hamada.

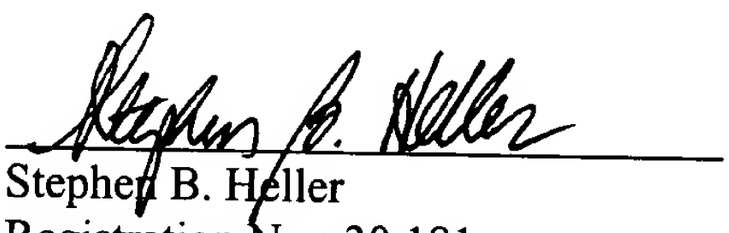
With respect to the Examiner's rejection under 35 U.S.C. 103, Hamada does not regard a hole in the pixel electrode (anode 103) as a problem to be overcome. Consequently, there is no suggestion or motivation for combining Hamada and Wolf, which teaches the planarization of a ragged surface formed by stacking layers.

Additionally, Wolf teaches forming planarizing dielectric layers in order to prevent an electrical disconnection of metal lines in multi-level interconnect systems caused by an increase of a step-height with an increase of additional metal lines stacked on top of one another. In contrast, the rejected claims recite a pixel electrode comprising an electrode hole which is filled up with an insulator comprising an organic resin in order to prevent a formation of a hole in an EL layer, thereby ultimately preventing an electrical shorting of an anode and a cathode sandwiching the EL layer. Consequently, Applicant submits that even if the teachings of Wolf were combined with Hamada, the structure recited in the claims would not be achieved.

Additionally, the rejected claims recite filling an electrode hole, namely a recess portion, that is both locally and particularly formed within the pixel electrode. None of Hamada, Wolf, and Kobayashi, et al. teaches this feature. Consequently, Applicant submits it would not have been obvious to achieve the claimed invention by combining the teachings of these three references.

In view of the foregoing amendment and remarks, Applicant respectfully submits that the application is now in condition for allowance, and an early Office Action in this regard is earnestly solicited.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

5. (Currently Amended) A self-light-emitting device comprising:

a plurality of TFTs;

a plurality of pixel electrodes over said TFTs;

a light emitting layer over said pixel electrodes; and

a cathode over said light emitting layer,

wherein said pixel electrodes are connected to said TFTs, respectively, ~~and~~

wherein a plurality of said pixel electrodes are formed in a pixel portion and an insulator is formed in each space between said pixel electrodes, and

wherein a thickness of a portion of the insulator higher than a top surface of the pixel electrodes is 0.1 to 1μm.

22. (Currently Amended) A self-light-emitting device comprising:

at least first and second switching elements;

at least one interlayer insulating film formed over said first and second switching elements;

at least first and second pixel electrodes formed over said interlayer insulating film wherein said first and second pixel electrodes are electrically connected to said first and second switching elements, respectively;

an insulating layer formed in a gap between said first and second pixel electrodes;

a light emitting layer formed over said first and second pixel electrodes and said insulating layer; and

a third electrode formed over said light emitting layer opposed to said first and second pixel electrodes,

wherein a thickness of a portion of the insulating layer higher than a top surface of the pixel electrodes is 0.1 to 1μm.